

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): ABE et al.	Atty. Dkt.: 01-519
Serial No.: Unknown	Group Art Unit:
Filed: Concurrently herewith	Examiner:
Title: VOLTAGE BOOSTER HAVING NOISE REDUCING STRUCTURE	

Commissioner for Patents
Arlington, VA 22202

Date: November 20, 2003

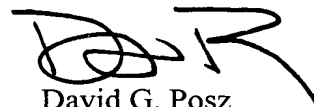
INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §1.56, the reference(s) listed on the attached Form PTO-1449 is/are submitted for consideration by the Examiner without any admission that it/they constitute(s) statutory prior art, or without any admission that it/they contain(s) subject matter that anticipates the invention or renders the invention obvious to a person of ordinary skill in the art.

The Examiner is requested to initial the attached PTO Form-1449 and to return a copy of same to the undersigned attorney as proof that the listed reference(s) has/have been considered and made of record.

Respectfully submitted,



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FORM PTO-1449	ATTY. DKT NO.	01-519	SER. NO.
	APPLICANT	ABE et al.	
	FILING DATE	November 20, 2003	GROUP

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
		6,469,569 (English counterpart of JP-A-2001-69747 which is discussed in page 2 of the spec.)	Oct. 22, 2002	Miyamitsu		
		2003/0085755 A1	May 8, 2003	Miyamitsu et al.		

FOREIGN PATENT DOCUMENTS

								TRANSLATION	
		DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS	YES	NO

* Full English text is available in machine-translated form in JPO (Japanese Patent Office) English language web site at <http://www1.ipdl.jpo.go.jp/PA1/cgi-bin/PA1INDEX>.

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

		John F. Dickson, "On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique", <u>IEEE Journal of Solid-State Circuits</u> , June 1976, pp.1-6 (discussed in page 3 of the spec.)
EXAMINER		DATE CONSIDERED